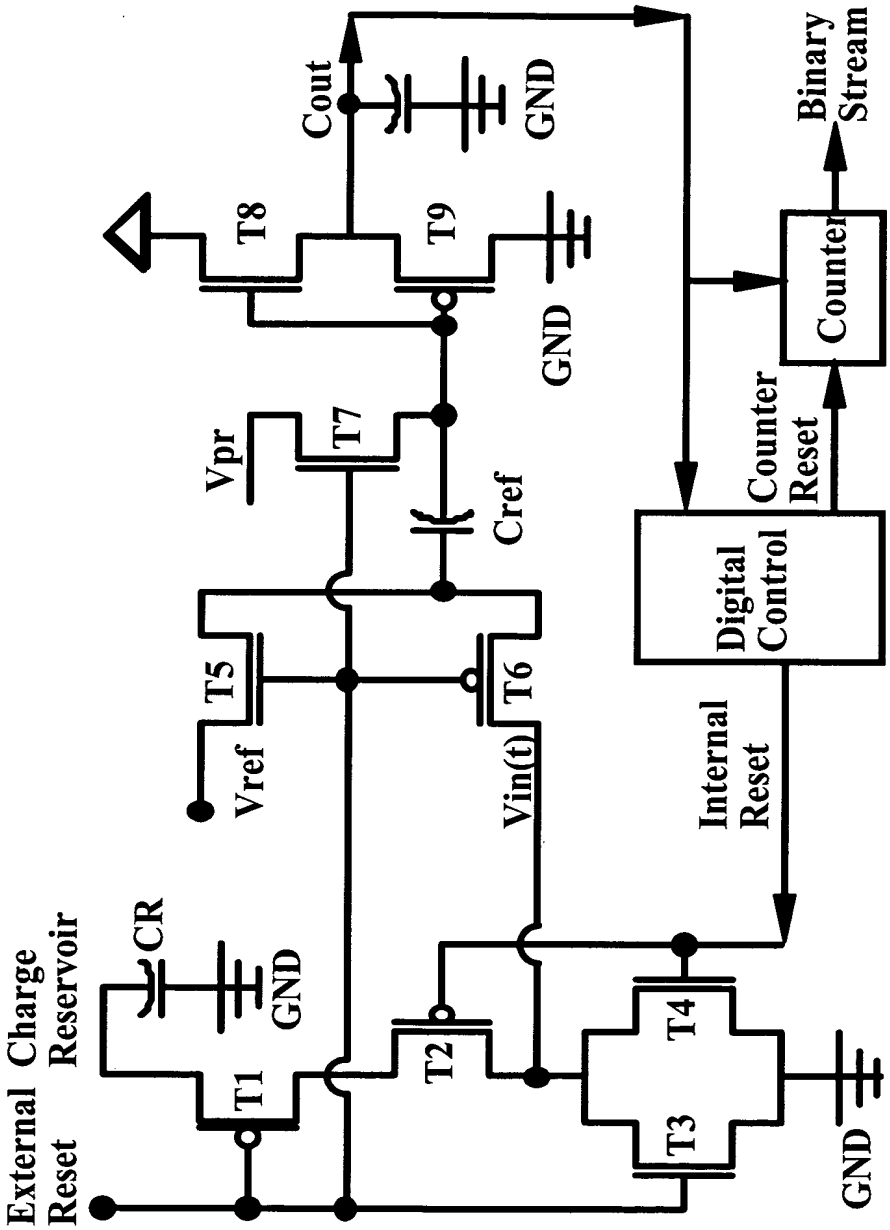
Figure 1


External Reset
Charge Reservoir
CR
GND
T1
T2
T3
T4
GND
Vref
T5
T6
Vin(t)
Internal Reset
Vpr
T7
Cref
T8
T9
Cout
GND
GND
Digital Control
Counter Reset
Counter
Binary Stream

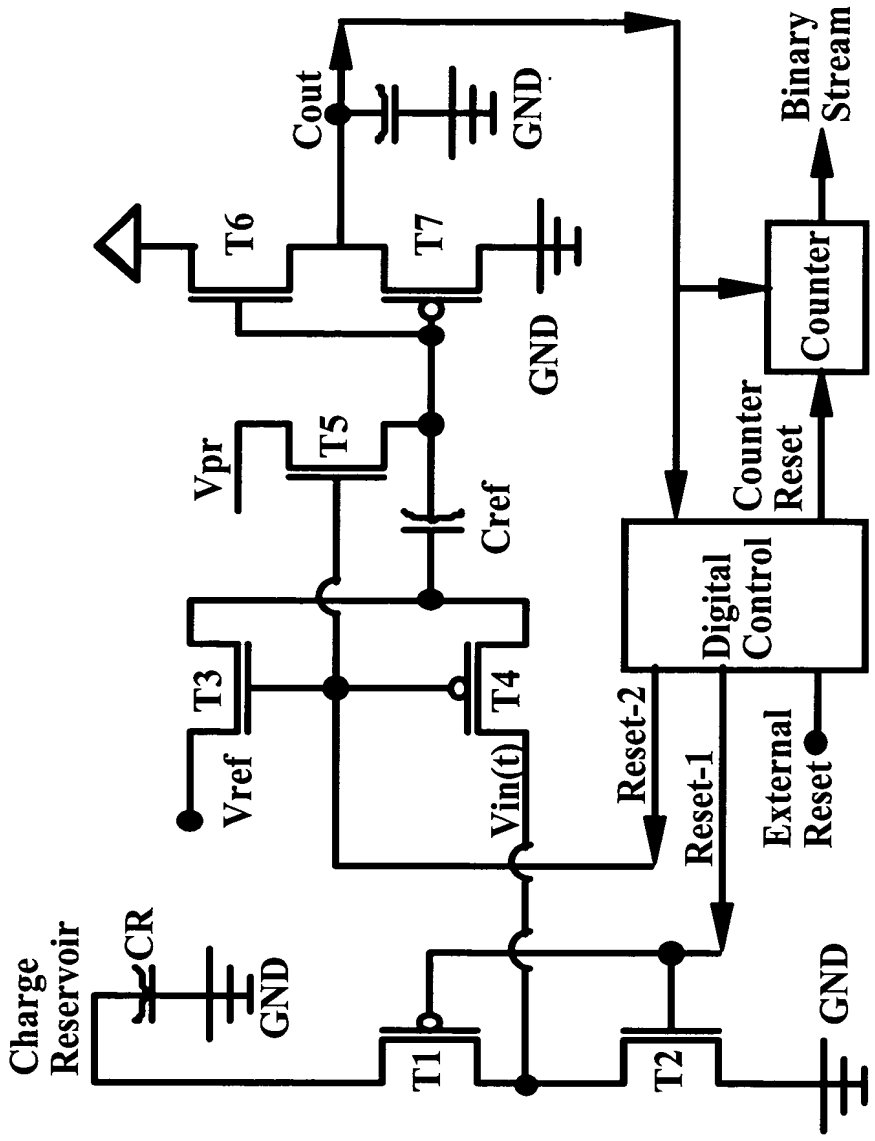

Cout
GND
Binary Stream
T6
T7
Counter
GND
Vpr
T5
Cref
Counter Reset
Digital Control
T3
T4
Vref
Vin(t)
Reset-2
Reset-1
External Reset
Charge Reservoir
CR
GND
T1
T2
GND

Figure 2

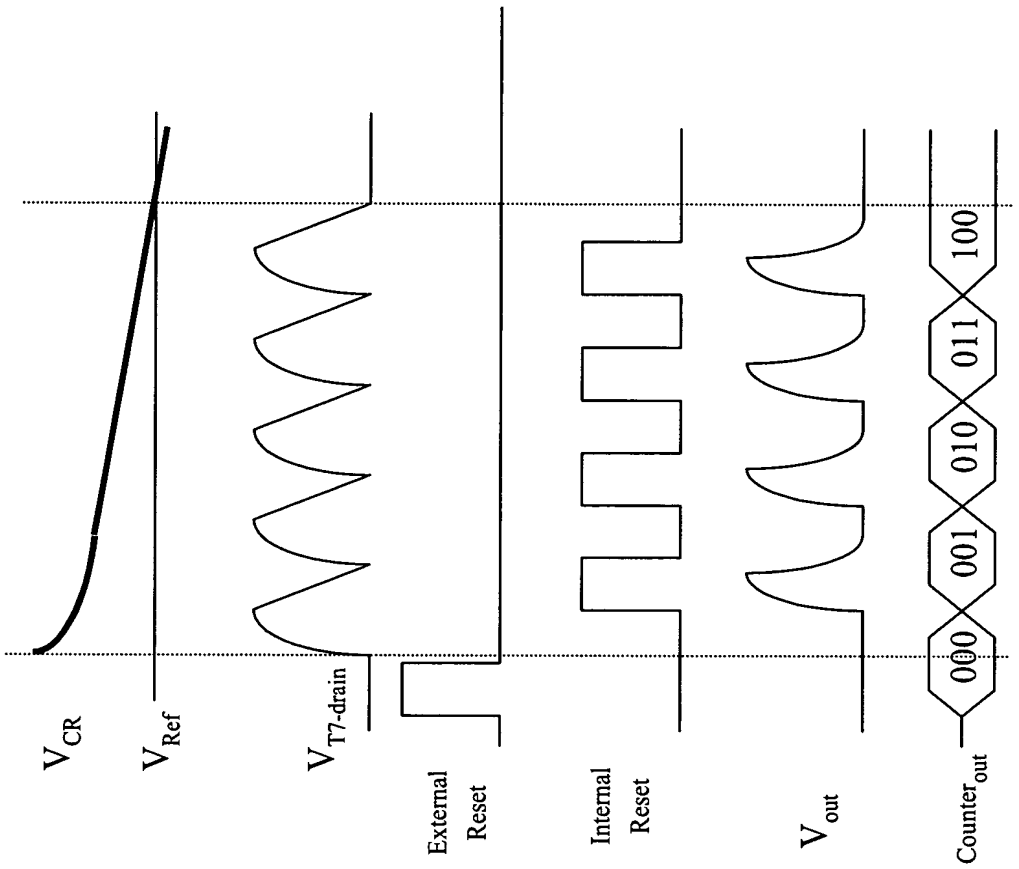

V_{CR}
V_{Ref}
$V_{T7\text{-}drain}$
External Reset
Internal Reset
V_{out}
$Counter_{out}$
000
001
010
011
100

Figure 3

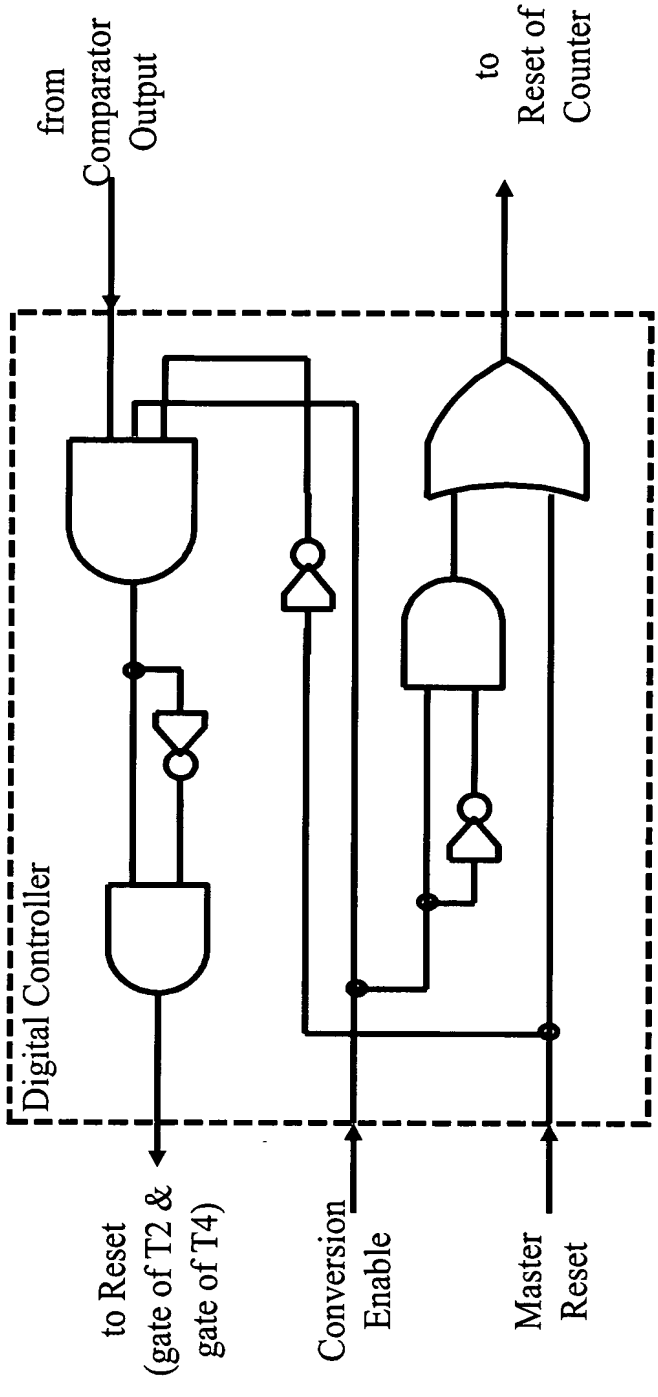

from Comparator Output
to Reset of Counter
Digital Controller
to Reset (gate of T2 & gate of T4)
Conversion Enable
Master Reset

Figure 4

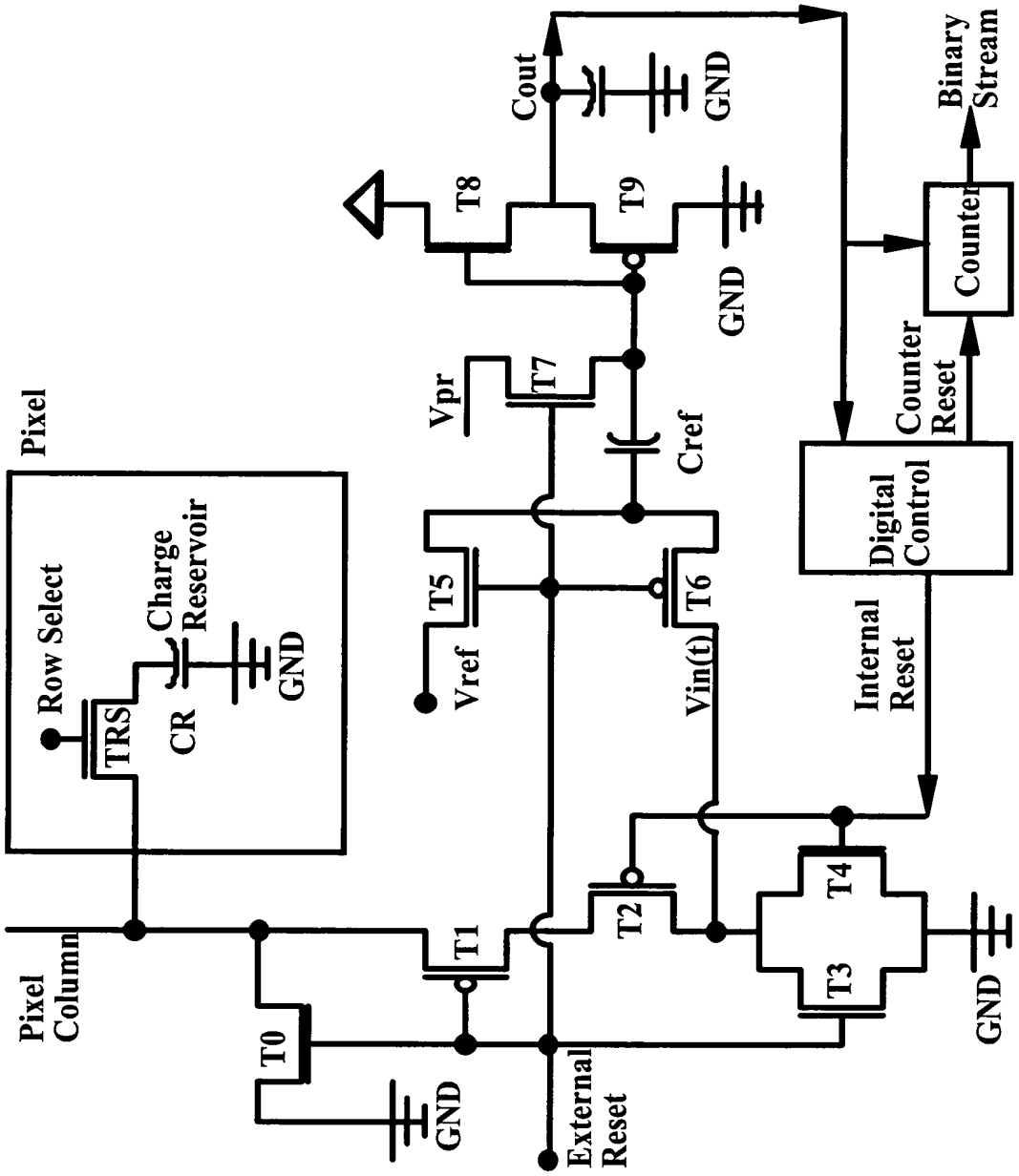

Pixel
Row Select
TRS
Charge Reservoir
CR
GND
Pixel Column
T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
Vpr
Cref
Vref
Vin(t)
Cout
GND
External Reset
Internal Reset
Digital Control
Counter Reset
Counter
Binary Stream

Figure 5

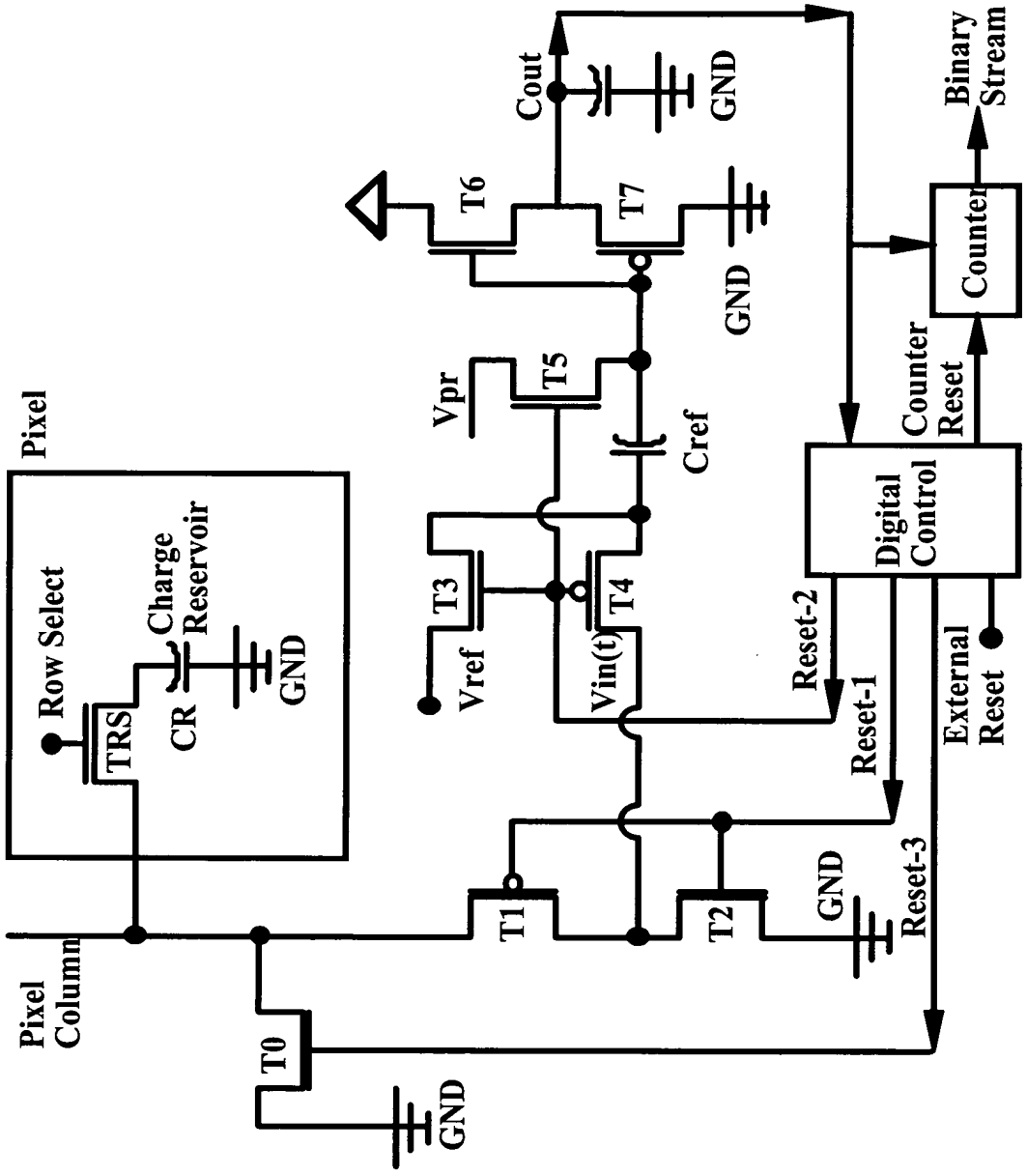

Pixel
Row Select
TRS
Charge
Reservoir
CR
GND
Pixel
Column
T0
GND
T1
T2
GND
Reset-3
Reset-1
Reset-2
External
Reset
Digital
Control
Counter
Reset
Counter
Binary
Stream
T3
Vref
T4
Vin(t)
Vpr
T5
Cref
T6
T7
GND
Cout
GND

Figure 6

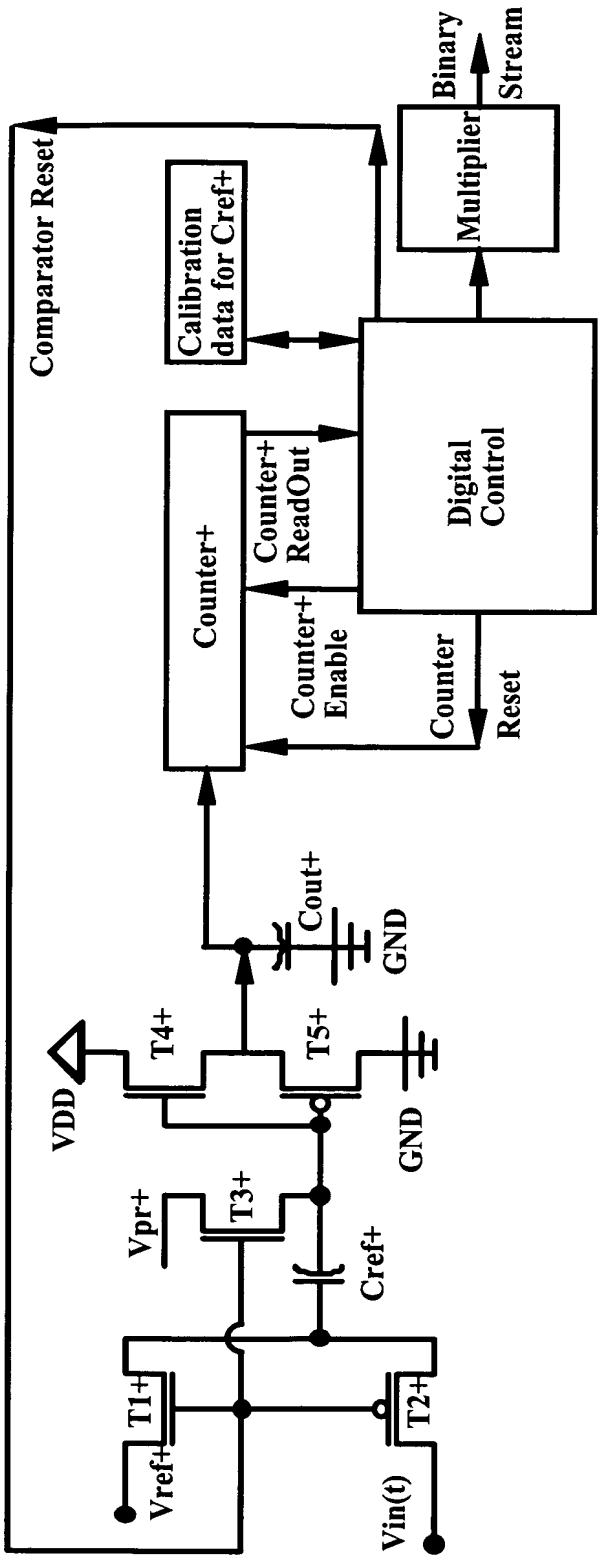
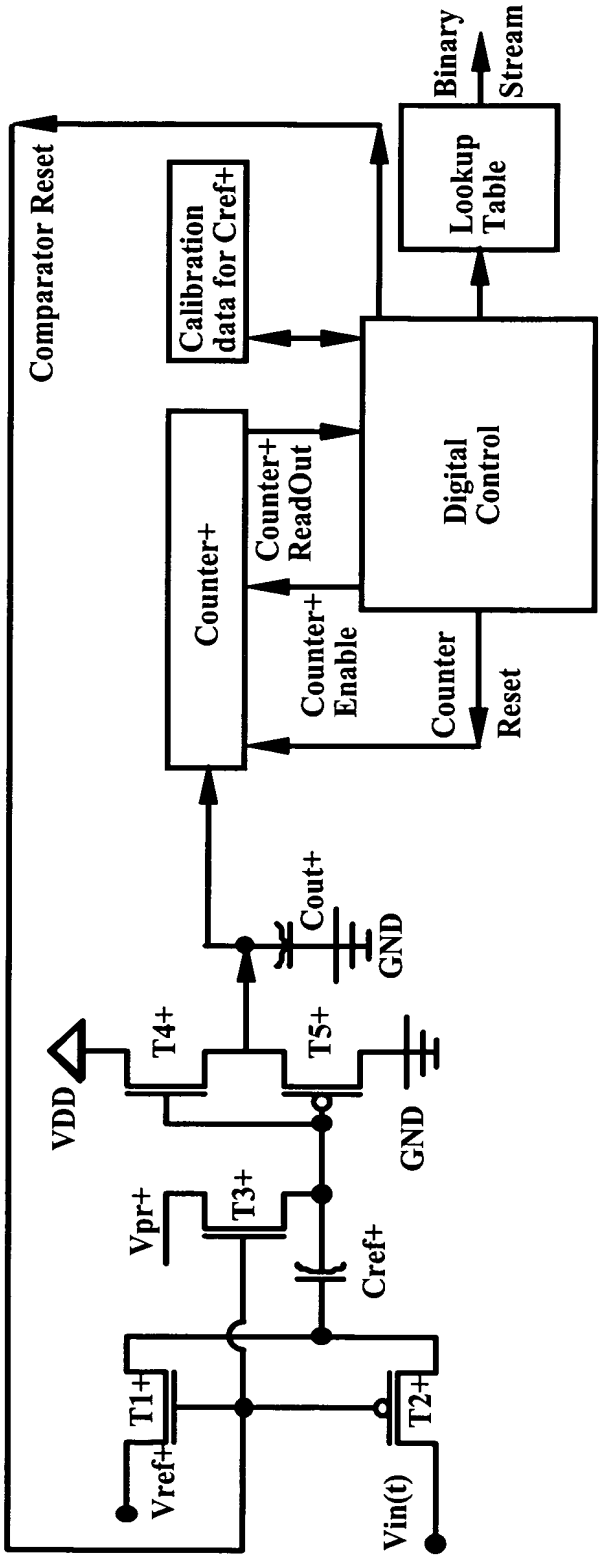


Figure 7

Figure 8



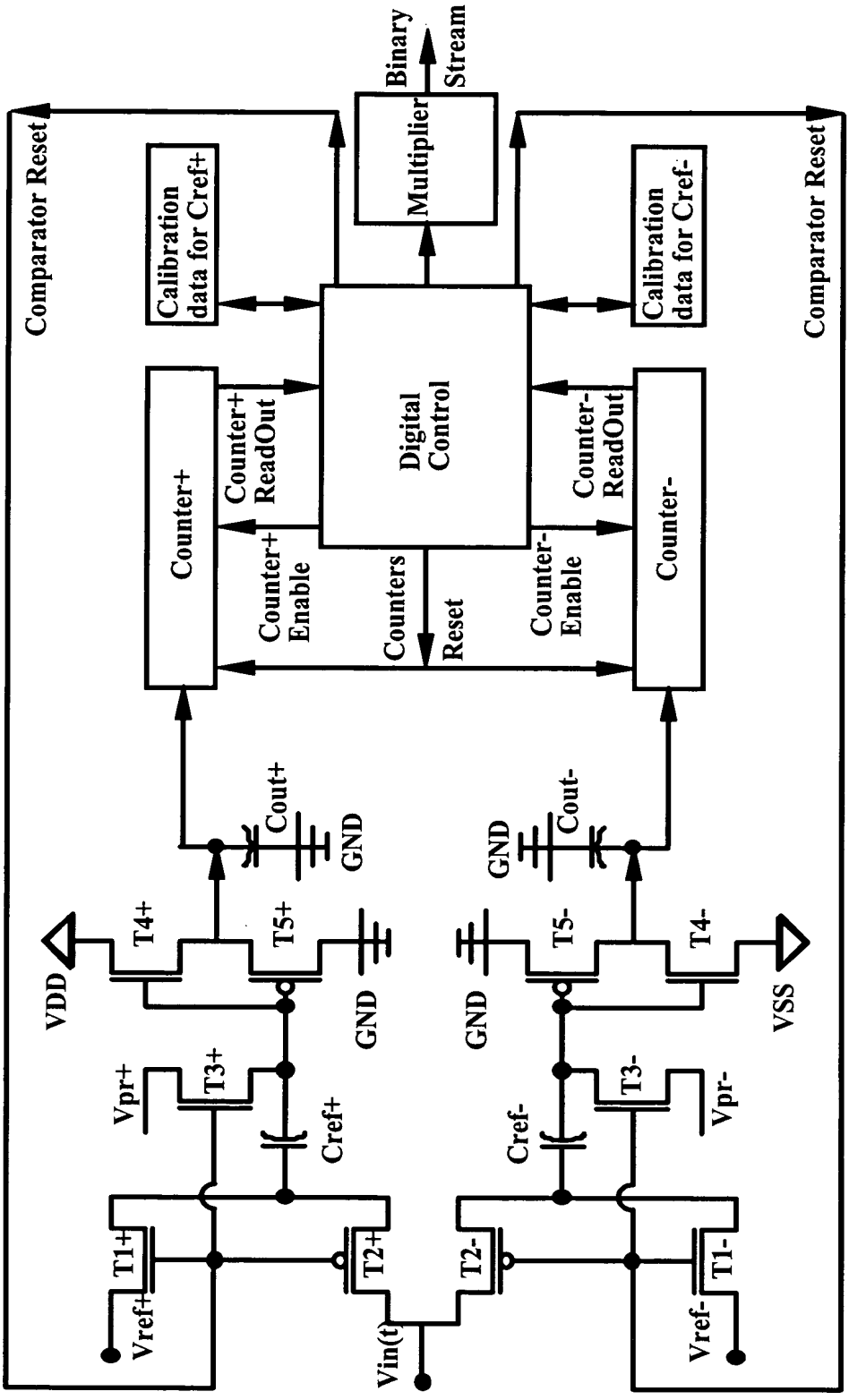

Binary Stream
Multiplier
Comparator Reset
Calibration data for Cref+
Calibration data for Cref-
Comparator Reset
Digital Control
Counter+
Counter+ ReadOut
Counter+ Enable
Counters Reset
Counter- Enable
Counter- ReadOut
Counter-
Cout+
GND
GND
Cout-
VDD
T4+
T5+
GND
GND
T5-
T4-
VSS
Vpr+
T3+
Cref+
Cref-
T3-
Vpr-
T1+
Vref+
T2+
Vin(t)
T2-
T1-
Vref-

Figure 9

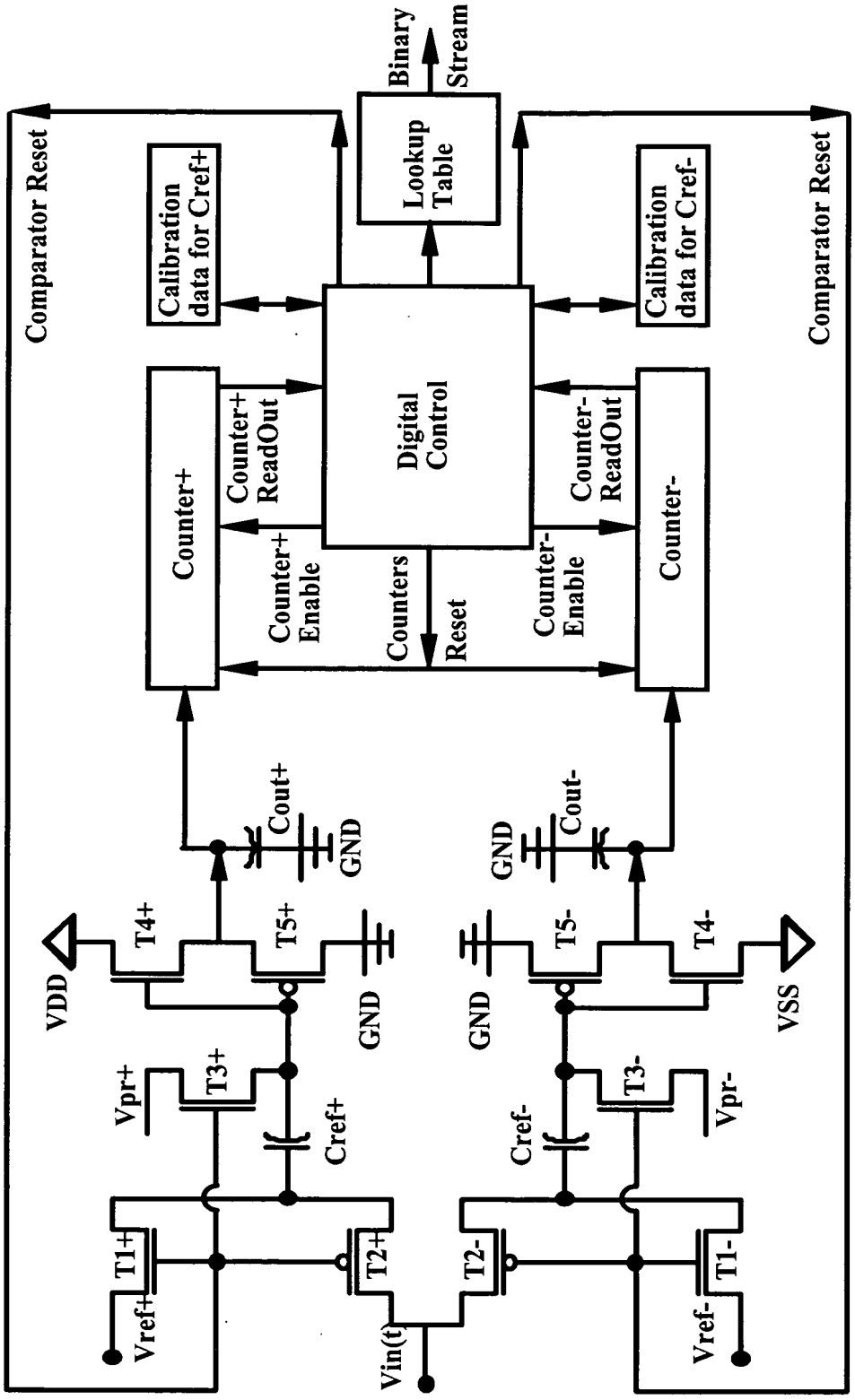

Binary Stream
Lookup Table
Comparator Reset
Calibration data for Cref+
Calibration data for Cref-
Digital Control
Counter+
Counter+ ReadOut
Counter+ Enable
Counters Reset
Counter- Enable
Counter- ReadOut
Counter-
Cout+
GND
Cout-
VDD
T4+
T5+
T5-
T4-
VSS
Vpr+
T3+
Cref+
Cref-
T3-
Vpr-
T1+
Vref+
T2+
Vin(t)
T2-
T1-
Vref-

Figure 10

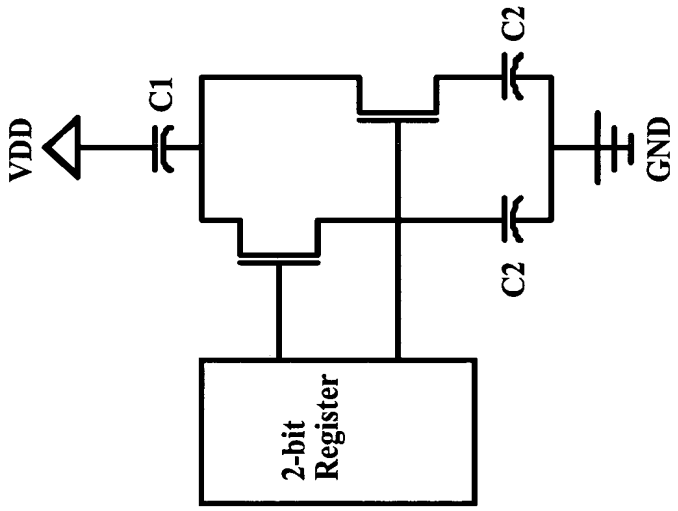


Figure 11

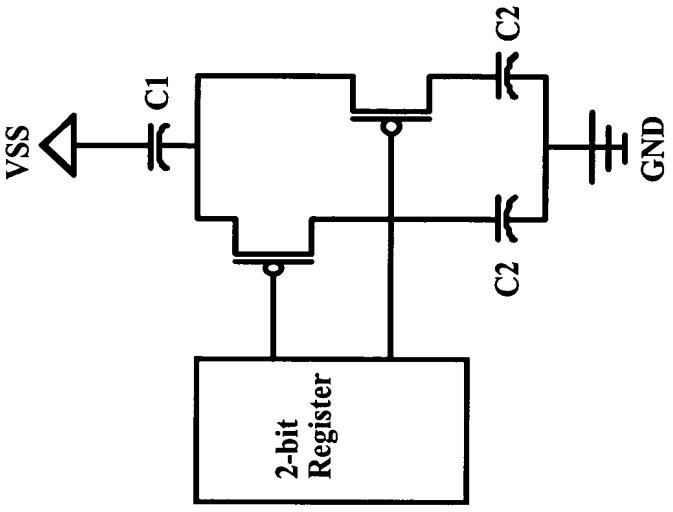


Figure 12

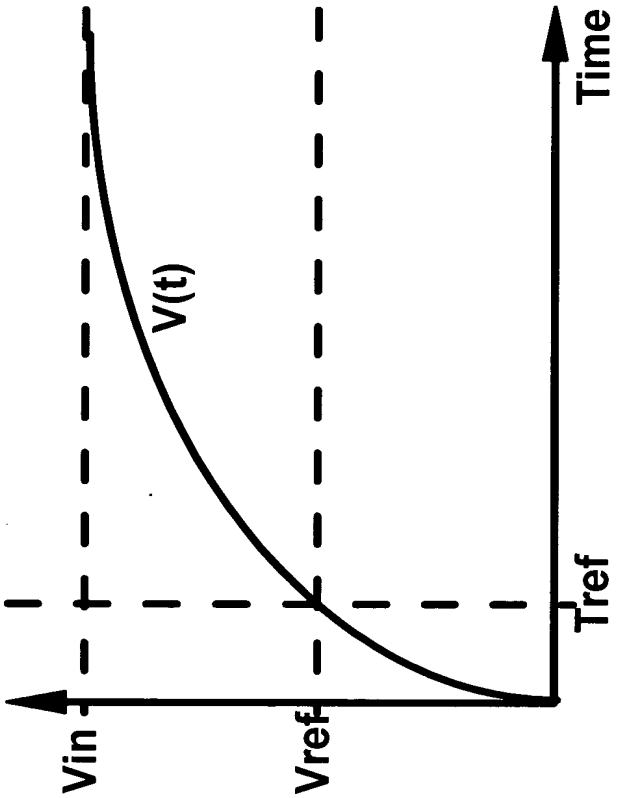


Figure 13

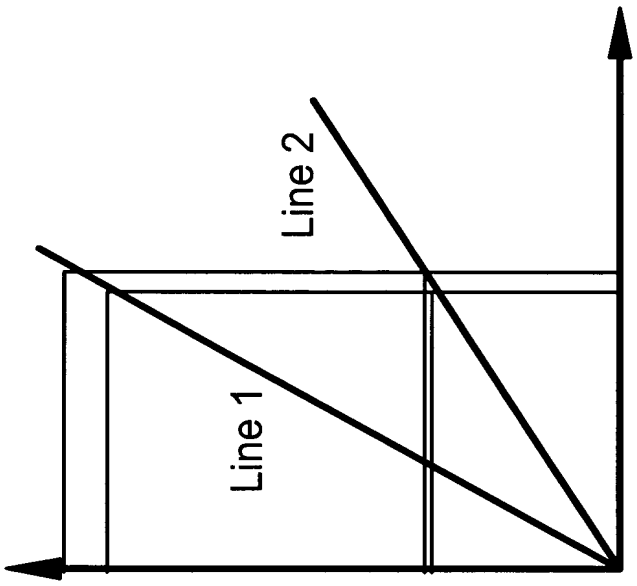


Figure 14

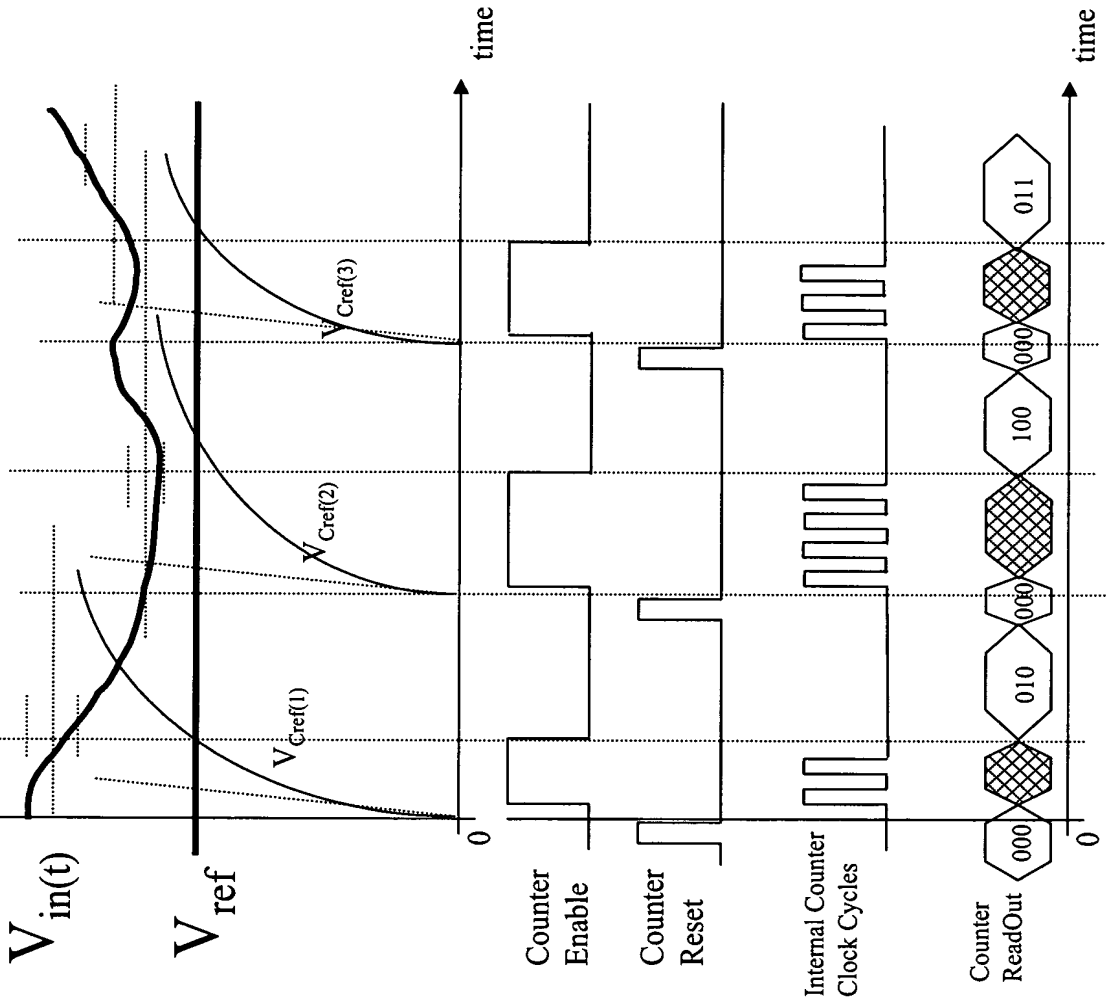

time
$V_{in(t)}$
V_{ref}
$V_{Cref(3)}$
$V_{Cref(2)}$
$V_{Cref(1)}$
0
Counter Enable
Counter Reset
Internal Counter Clock Cycles
Counter ReadOut
000
010
000
100
000
011
time
0

Figure 15

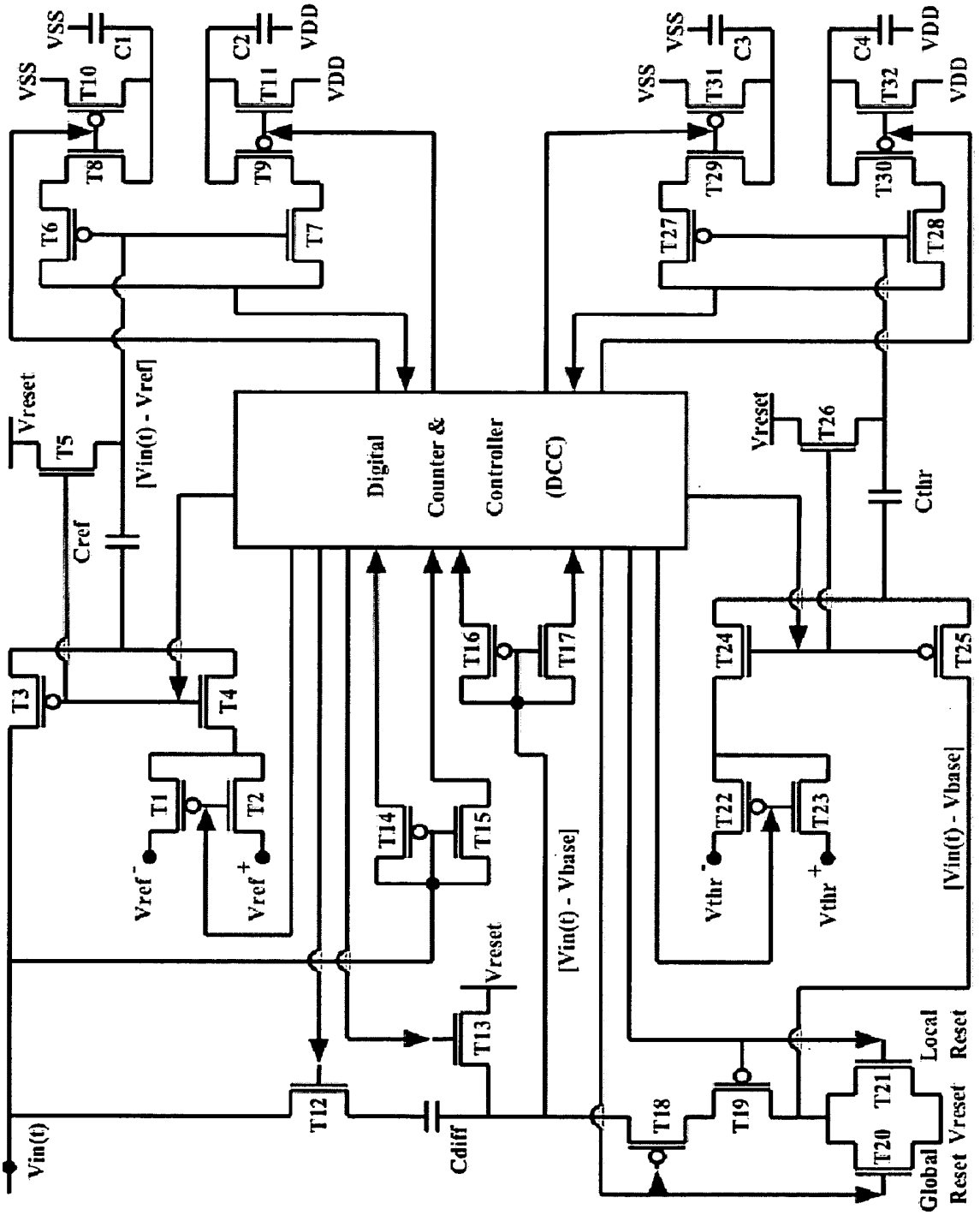

VSS
C1
C2
VDD
C3
C4
T10
T11
T31
T32
T8
T9
T29
T30
T6
T7
T27
T28
Vreset
T5
[Vin(t) - Vref]
Digital
Counter &
Controller
(DCC)
T26
Cthr
Cref
T3
T4
T16
T17
T24
T25
T1
T2
T14
T15
T22
T23
Vref -
Vref +
Vthr -
Vthr +
[Vin(t) - Vbase]
T13
T12
T18
T19
T21
T20
Local
Reset
Global
Reset
Vin(t)
Cdiff

Figure 16

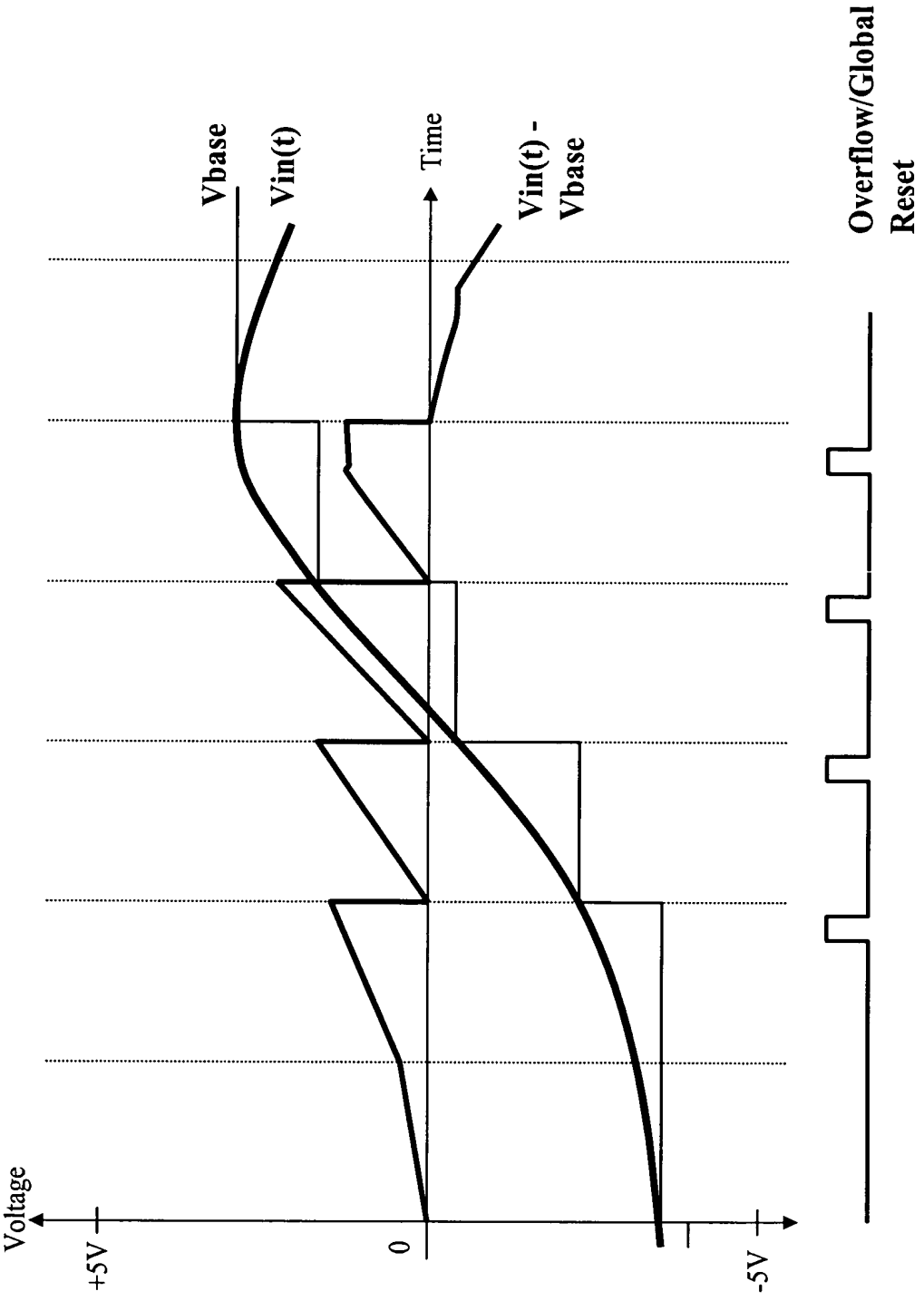

Vbase
Vin(t)
Time
Vin(t) -
Vbase
Overflow/Global
Reset
Voltage
+5V
0
-5V

Figure 17

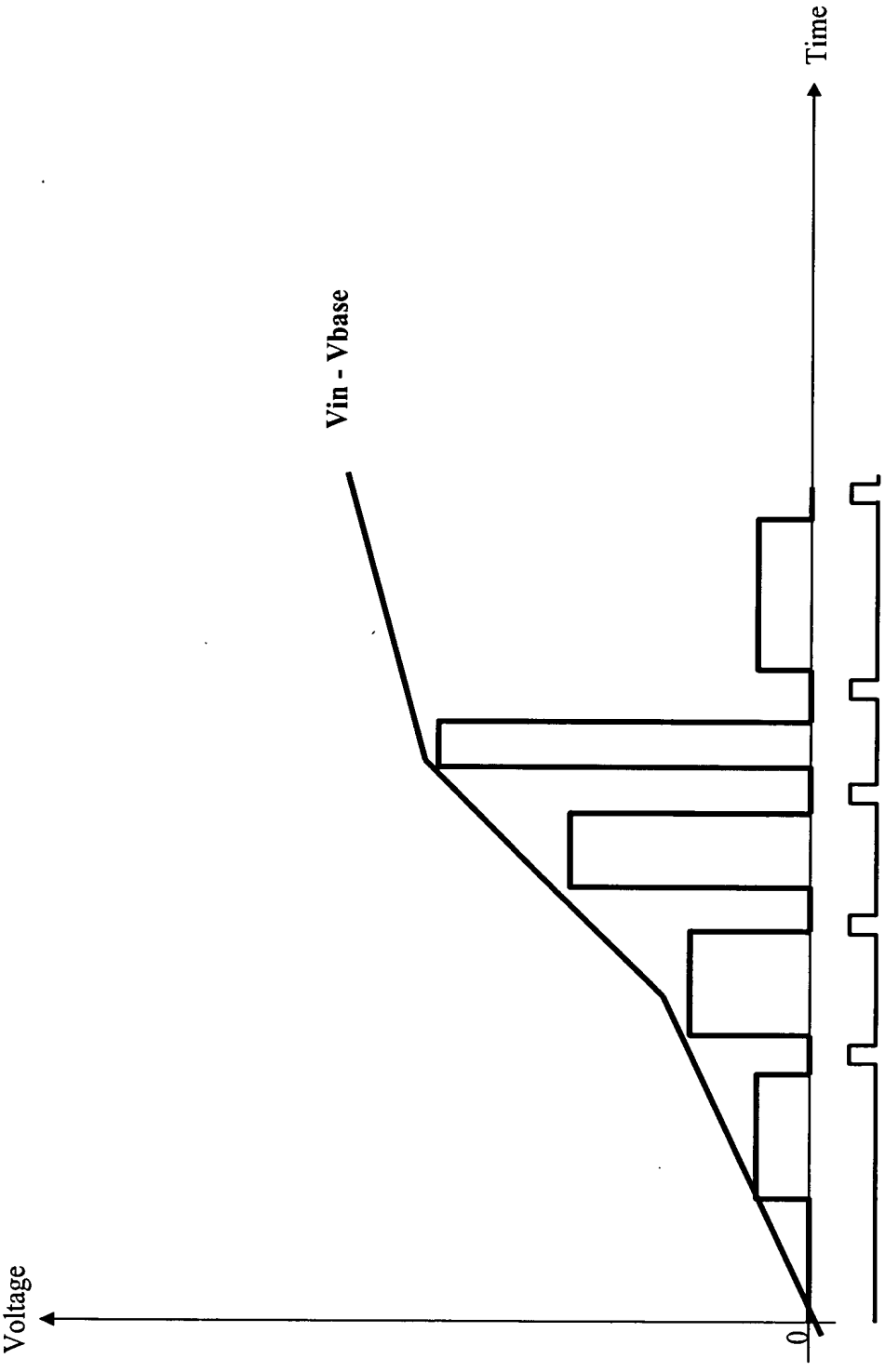


Figure 18